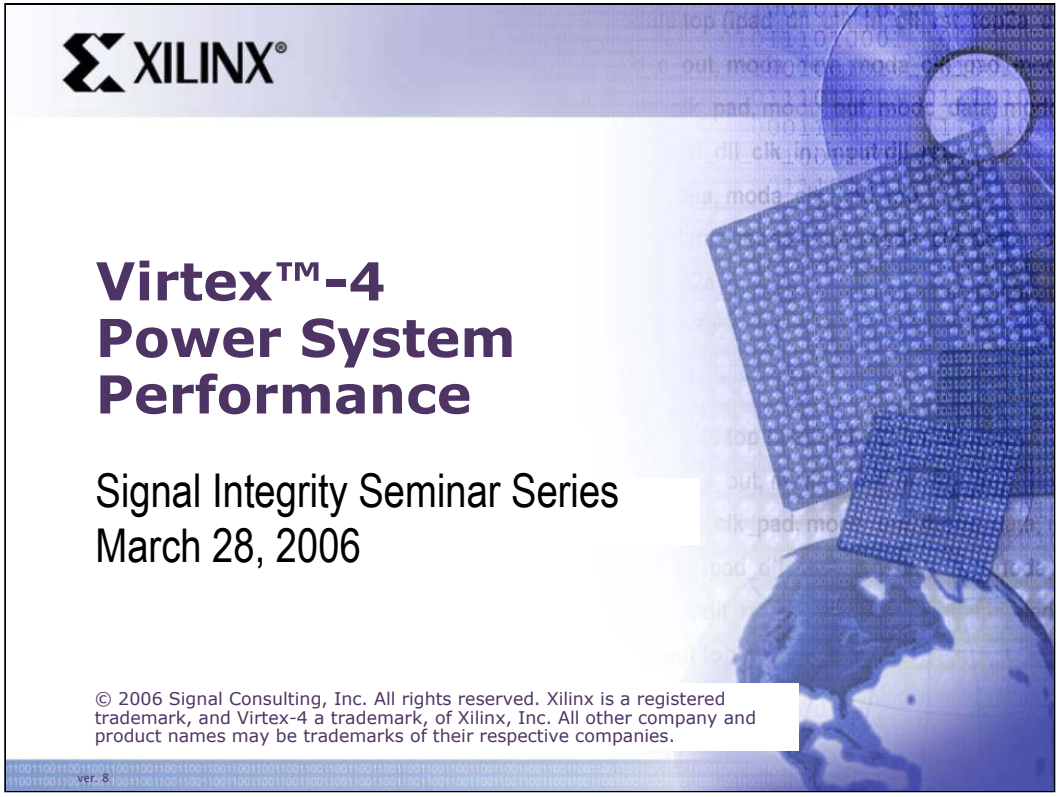
Welcome to Part I of "Power System Analysis", brought to you by Xilinx.

My name is Mark Alexander, I'm an application engineer. I specialize in the Virtex product family.

In my job, I spend a lot of time helping people with their pcb power architecture. Power is becoming an increasing problem, especially given the proliferation of different power supply voltages.

To help me better understand how power systems function, I've recently undertaken some measurements on working FPGA designs, and would like to share with you today the results of that work.



In preparing this seminar I've had the pleasure of working with two people who are experts in their fields. The first, Michael Brenneman is the director of packaging and pcb at Ansoft Corporation. He has done some stunning simulation work for this project that I think you will enjoy seeing.

The second person is the author of the popular book "High-Speed Digital Design", the signal integrity columnist for EDN magazine, and a frequent guest lecturer at Oxford University,

Please join me in welcoming our speaker for today, Dr. Howard Johnson.

Introduction

Mark Alexander
Product Application Engineer
Xilinx, Inc.

Michael Brenneman
Director, Packaging and PCB
Ansoft Corporation

Everybody needs a good power system

- But what is "good"?
- How is it measured?

Thank you, Mark, for that introduction.

I have had a great time working with both you and Michael for this presentation.

Every PCB has a power system, put together usually from a conglomeration of multiple (sometimes conflicting) requirements taken from many sources, plus a dash of experience based on what worked last time.

If a power system didn't occupy much board area, or cost very much, or all those vias didn't wipe out so many signal routing channels within your board, none of us would care.

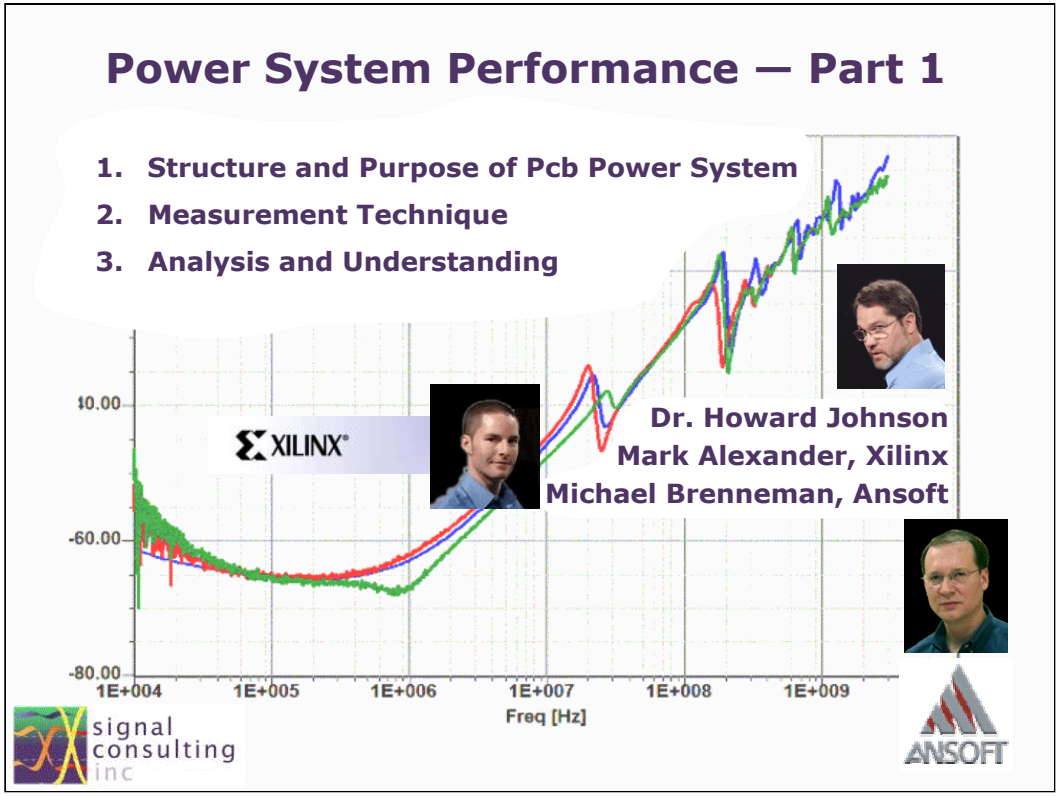
Since, at least in the designs I look at, power systems are looking more and more onerous each year, I think it would be helpful to examine three main topics taken from my recent work with Xilinx and Ansoft:

First: Structure and purpose of a pcb power system. This is understood to be in the context of a high-speed digital system with solid power and ground planes.

Then: Power system measurement technique. Contrasting what you *want* to measure with what you CAN measure.

Finally: Analysis of results. Leading to a better understanding of BGA package performance.

All the examples will be taken from a Virtex-4 application board called the ML-405. I have a picture of one right here.



It’s a typical board. You can see the big Virtex-4 FPGA right in the middle. This card contains just about one of every type of high-speed interface. It’s a demonstration board. Starting from the FPGA location, if you go above and just to the right of the FPGA the next big chip is a DDR SDRAM. There are two of those on this board, one on the top side and one on the back. The path from FPGA to SDRAM is 32 bits wide.

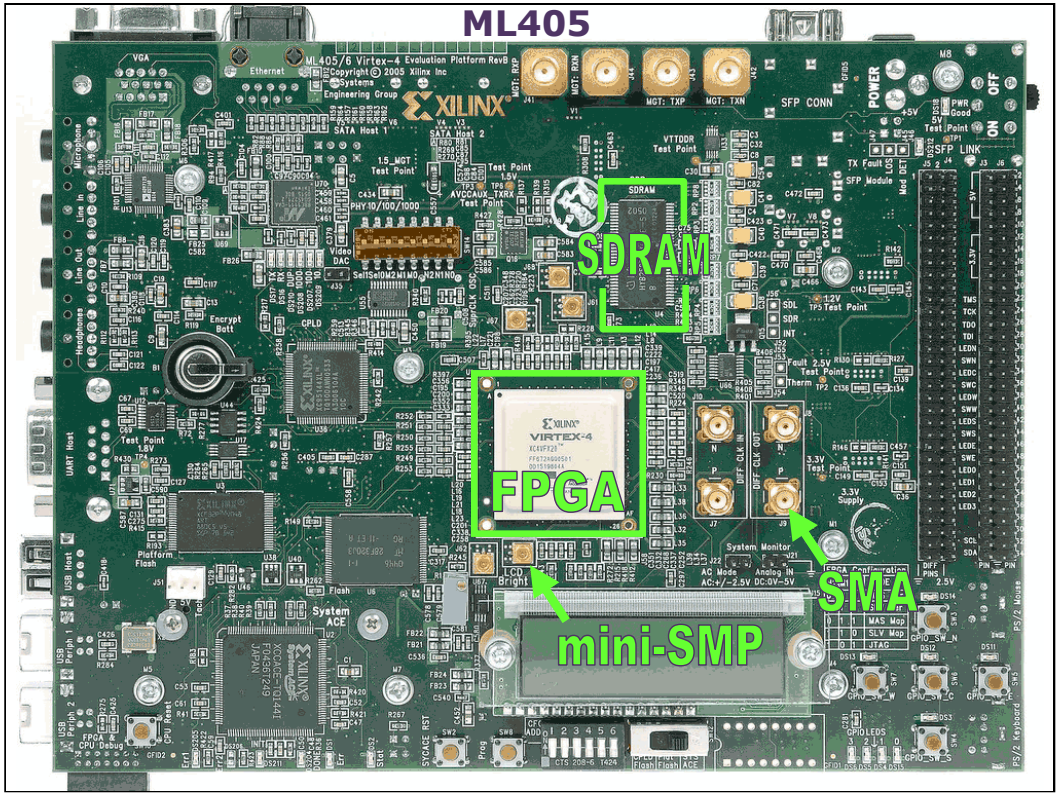
You can see we have instrumented the card with a lot of RF connectors. These hook to the power planes inside the card. We will use them to probe the power system.

The next slide depicts the power delivery system on this card.

Every practical power system comprises several stages of power delivery. Each stage acts as a filter. The filters operate at different frequencies.

Each filter network exists to provide a low-impedance path from local VCC to local ground, but because of the internal parasitics of the components used (particularly the unavoidable parasitic series inductance), each filter only works over a limited range of frequencies.

Generally speaking, the larger components operate at lower frequencies.



In this example,

(1) The relatively large components in the VRM circuit operate at the lowest frequencies, from sub-hertz up to a few kHz. The bulk decoupling capacitor, sometimes considered a part of the VRM, operates in the tens to hundreds of kilohertz arena.

(2) A distributed array of surface-mounted bypass capacitors works from a megahertz up to easily a hundred megahertz. In conjunction with tightly-spaced planes the pcb system can work to 500 MHz or more.

(3) The tiny planes, and very low-inductance capacitors in a BGA package can be effective at frequencies even higher than a pcb.

(4) Finally, above a GHz, the capacitance of the die becomes extremely important.

Working together all four pieces of your power system act to provide a low impedance between local VCC and local ground, at all frequencies of interest, *everywhere you need it*.

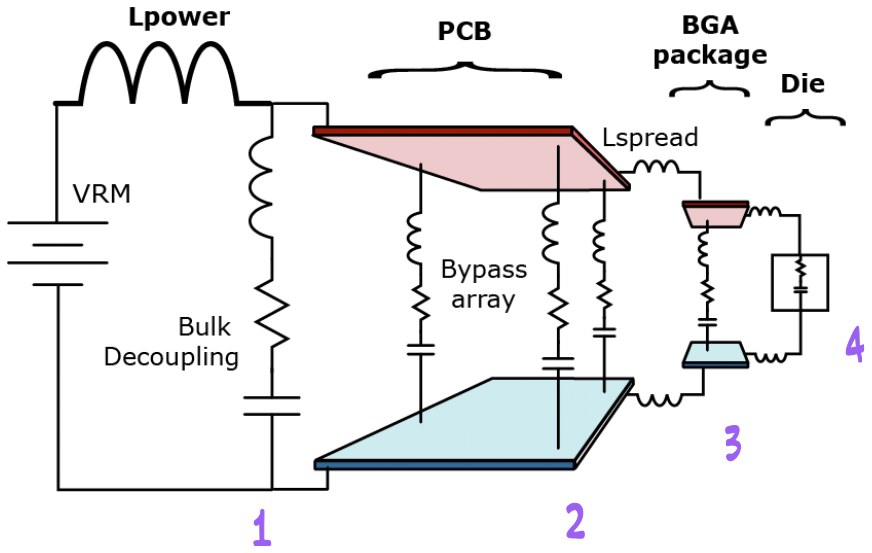
I emphasize that last point, "everywhere you need it", because it turns out that you do **not** need a low-impedance connection from power to ground absolutely everywhere.

Let's look in detail at the places where you **DO** need low-impedance connections between power and ground.

The next slide shows the complete path of current in a high-speed signaling application.

Suppose a signal source (on the left of the diagram) switches HIGH. Current flows out the I/O pin, across the pcb on a trace and then to a load.

Structure of Power System



A digital power system cascades four distinct filter networks.

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That's only half the story. As your signal propagates, current builds in a path along the reference plane underneath your trace. By the time your signal edge arrives at the end termination, you have built up a complete round-trip pathway from source, through the load, and back to the source. Both outgoing and return pathways are needed to propagate digital signals. To complete the flow of current, you need low-impedance inter-plane connections in three places:

At signal sources: An integrated circuit with single-ended outputs acts much like a current source at the die location, demanding surges of current from your power distribution network. If the power network collapses too far when demanding current, the chip can't work.

The key parameter that determines the amount of rail collapse at the die is the impedance of the power distribution network, as seen by the die, at the die location.

At signal loads: If you have a bank of split terminations, the aggregate signal current from all lines flows into the power and ground planes at that point. You need a low impedance power-ground connection at the terminator location to control noise (crosstalk) within the termination network.

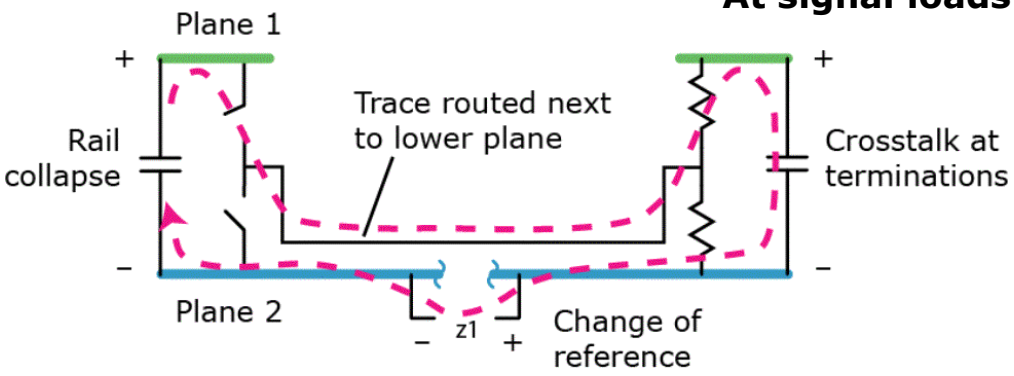
Where traces change reference planes: If your trace switches layers from one reference plane to a different one, the two planes must be connected at that point.

Example: Suppose a trace runs along next to plane 2 for a while, then hops to a new layer. The new layer lies adjacent to plane 3.
The next figure shows the equivalent circuits prevailing in the local vicinity of this hop.

Low-impedance Plane Connections Are Required in Three Places

At signal sources

At signal loads



Where traces change reference planes

The equivalent circuit model for the trace on the left as it approaches the hop is a voltage source with a 50-ohm output impedance, feeding the right-hand side of the circuit.

The equivalent model for the trace on the right, leading away from the hop location, is a 50-ohm load *not* going to "*ground*", but leading to plane 3, the new signal reference (i.e., nearest plane).

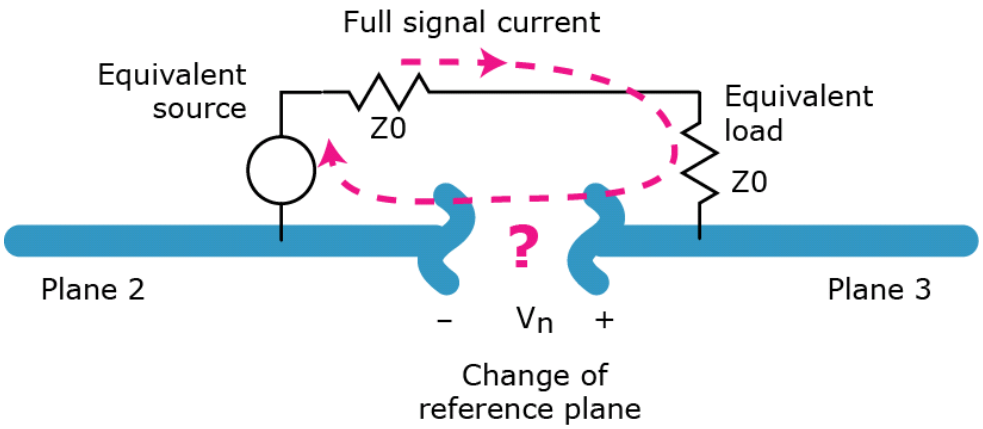
The far-end load doesn't matter for fast events. Right now, just as a fast edge traverses this structure, the signal sees only a 50-ohm load to plane 3. Signal current passing through this effective load impedance must return from plane 3 back to plane 2. How does the returning current leap across the inter-plane gap?? It flows through whatever impedance happens to be handy; perhaps a bypass capacitor, or the natural parasitic capacitance of the planes themselves. Whatever path the returning signal current takes, that path has some finite impedance. Call it Z[2,3].

As the returning signal current passes between the planes it generates a noise voltage V[n], equal to I[signal]*Z[2,3]. This noise voltage V[n] affects all other traces crossing the same chasm. This effect is a form of crosstalk.

The crosstalk noise from all traces crossing the same chasm aggregates. For example, if you get 4 mV noise plane-to-plane from a single trace crossing the chasm, then 100 traces doing this will generate 400 mV noise. Nasty.

To fix crosstalk from layer-changing structures, you must either add bypass capacitors in the vicinity of the layer-change to reduce the local impedance plane-to-plane in that area, or place your planes closer together, or DON'T CHANGE PLANES LIKE THAT.

Change of Reference Planes



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What I would like you to remember from this discussion is that good, low-impedance inter-plane connections are necessary in three places: signal sources, signal loads, and wherever traces change reference planes.

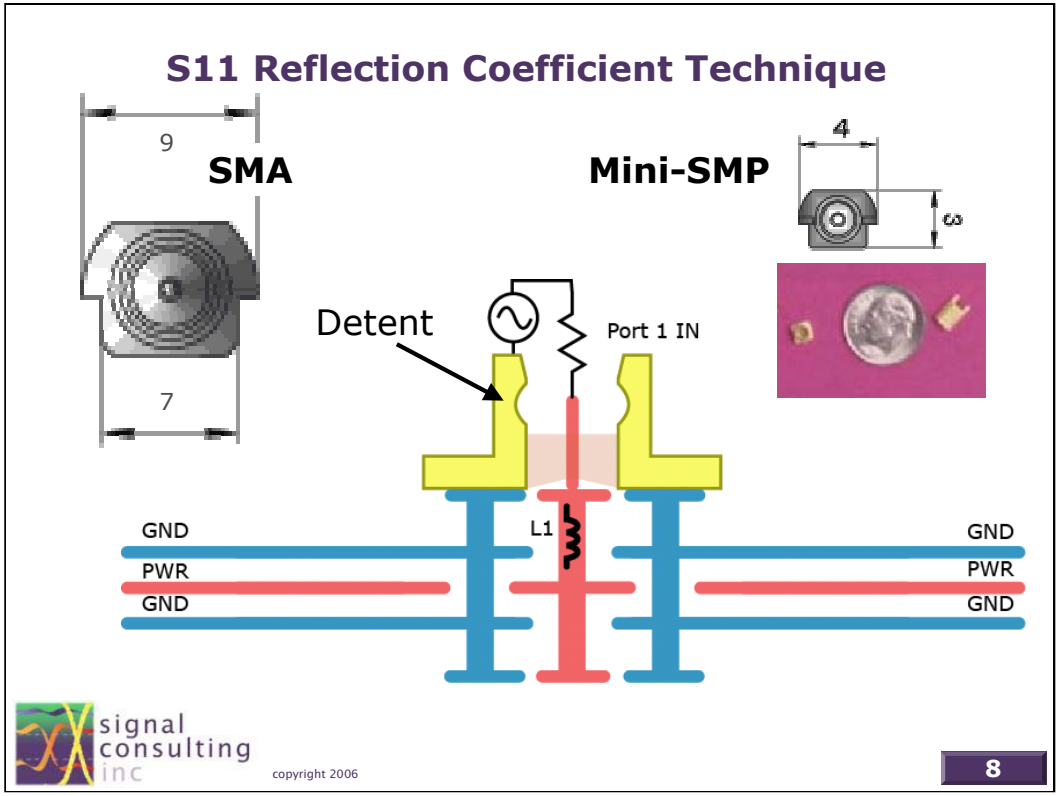
In all three cases we need a way to measure the impedance from plane to plane—let's look at that next. This picture illustrates a simple vector network analyzer (VNA) method that may occur to you.

In the figure I show an RF connector attached to a PCB (Rosenberger mini-SMP surface-mount PCB connector). This connector is very tiny and uses a detent system for connector alignment (no "screwing in" the connectors as with SMA types). I've labeled the connection "port 1" on the drawing.

You might hit on the idea of using a vector network analyzer (VNA) to measure the impedance at port 1. A good thought, but there is a problem with that method.

Franks Laws, in his book "Electrical Measurements", advises us that "It is important not to lose sight of the possible influence of the measuring instruments on the results." That statement is just as true today as is was in 1917 when Frank first wrote it. So, let's look at the parasitic effects in this measurement.

In any attachment, there is an unavoidable series inductance leading from the connector vertically down through the board stack to the power planes. This impedance acts in series with the power plane. It is very NOTICEABLE compared to, if not LARGER than the natural impedance of the power plane you plan to measure, and disturbs your measurement SIGNIFICANTLY.



Those of you familiar with "de-embedding" might attempt to design a reasonably-well-matched 50-ohm launch all the way down vertically through the board to the power plane, and then "de-embed" that stub (people do such things). Unfortunately, there is no way to physically calibrate this setup.

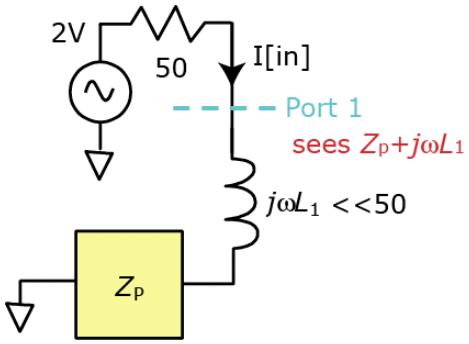
Here is another problem with the S11 technique. The measurement of very small impedances using an S11 reflection setup involves the computation of very fine difference between two large quantities: the signal going in, and the signal reflecting back. These two signals have almost exactly the same amplitude. For this reasons I recommend that you NOT use S11 reflection coefficient measurements for power-system impedance work.

A better technique is the S21 measurement, shown at right. In this setup port 1 sends and port 2 receives. Provided that impedances Z_p and $j\omega L_1$ remains small compared to 50 ohms, the transmitted current remains fixed. The signal amplitude at port 2 varies in almost direct proportion to Z_p. The constant of proportion for 50-ohm source and load impedance is shown in the equation. This technique is the modern equivalent of a "four-terminal resistor measurement".

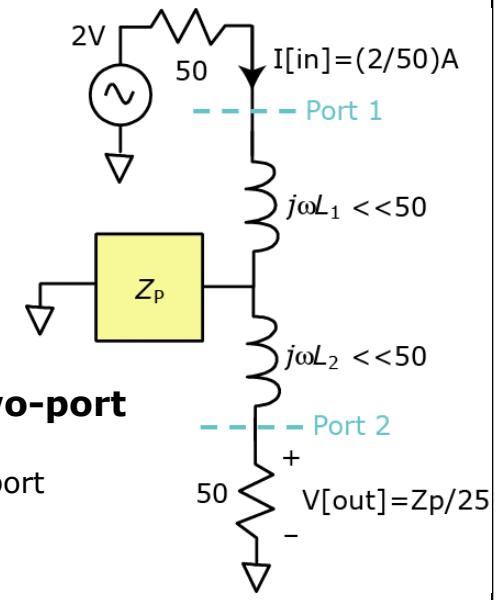
NOTE ABOUT PARASITICS: In the S21 measurement, L1 influences the amount of current supplied to the power plane only by the ratio (50)/(50+jwL1). For L1 equal to 400 pH (a worst-case value for a very poor layout) the effect of L1 amounts to only 0.1 dB all the way up to 3 GHz (as far as we went in these tests). L2 exerts a similarly small effect on the outcome.

SECOND NOTE: Parasitic capacitance in the connector matters even less—remember, you are hooking up to an unbelievably HUGE parasitic capacitor anyway.

Instrumentation Schematics



One-port



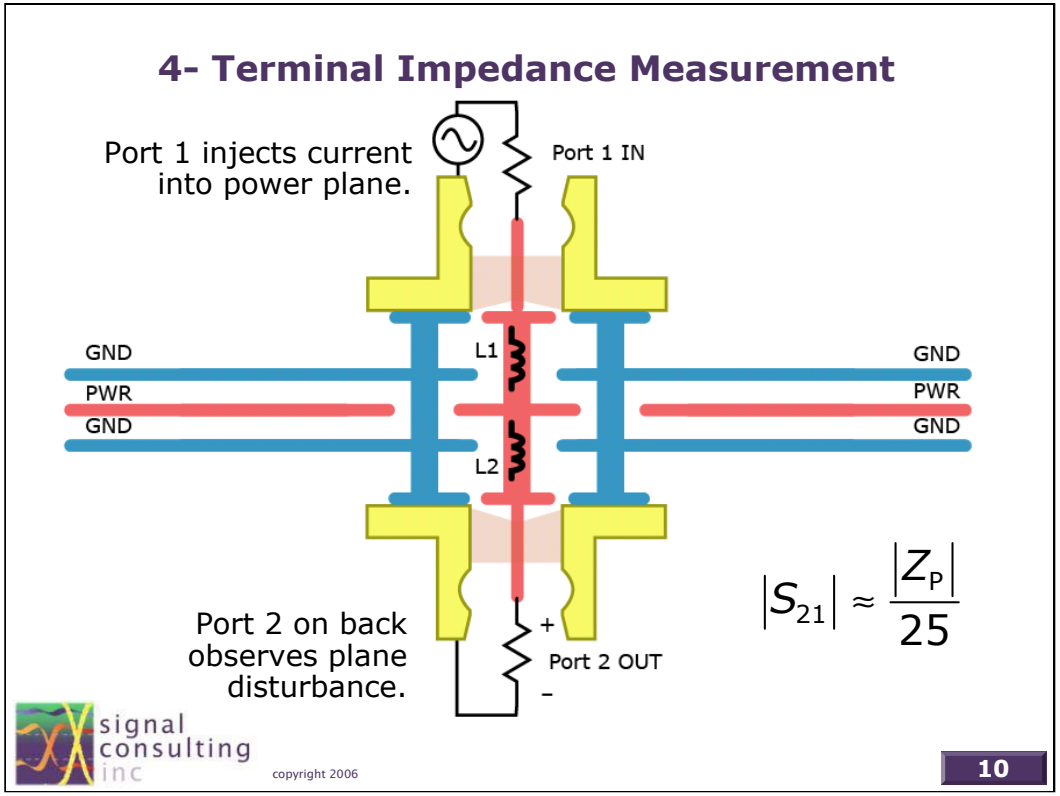
Two-port

L_1 interferes with one-port measurement.

Here is a layout view showing how the connectors are applied to the board. This technique requires surface-mounted connectors (Rosenberger mini-SMP).

Do not place the connectors near each other on the same side of the board. Crosstalk between the connectors will noticeably affect your signal readings. Remember, you are looking for *very tiny* impedances. The expected attenuation from one side of the board to the other may approach 80 dB. Even miniscule amounts of crosstalk disturb these readings.

Always position the connectors on opposite sides of the board.



The board stack-up comprises twelve layers, divided into six signal layers and six plane layers.

In the scanning-electron photomicrograph you can see the relative spacing of the layers. I like to look at layer stacks this way, showing the physical dimensions involved.

I colored the ground layers blue and the signal layers red in this drawing. Signal layers are green.

The 2.5-volt power plane, common to our FPGA and also the DDR SDRAM, resides on layer PWR6 (P6) *along with a slew of other voltages*. On this layer there are "patches" for VCCO power (IO bank 7), some gigabit Ethernet special power regions, and some other stuff. All the power layers are like that. I counted twelve different kinds of power and four different kinds of ground on this board. What a system! Every chip has its own recommendations for "what to do" for power, and the designer of this board just threw in everything that everyone asked for. As a result the power planes look like a map of the Balkans—a whole bunch of little-bitty regions all jammed together.

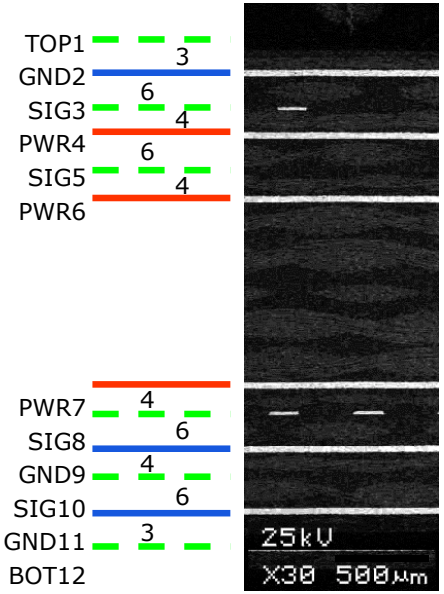
Not only that, but look at signal layer 5. It's totally confined between two power layers. Whatever power noise exists on those planes is going to couple directly to the traces on SIG5. Looking at it the other way, activity on the SIG5 trace layers couples noise into every power layer those traces pass by.

If noisy traces happen to pass adjacent to a sensitive, specially filtered power-plane region, you can bet that region won't be "quiet".

Board under test

www.caingram.info/Balkans/Pix/Map.jpg

Six signal layers, poor power architecture. Great example.



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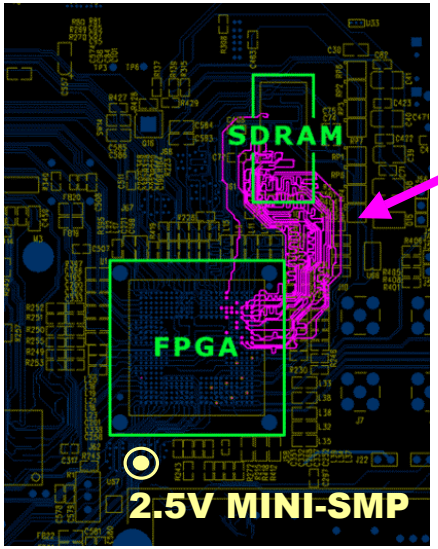
Guess which layer our SDRAM traces are on? This picture highlights (in purple) the SDRAM traces on layer 5. Half of them lie on layer 5, the other half on layer 8. I labeled these layers DDR5 and DDR8 in the layer stack drawing.

I'm getting interested in measuring crosstalk between the SDRAM traces and the 3.3V power supply region on layer 4. I won't have time to do that today, but maybe we can get to it later.

Crosstalk is mostly just a matter of proximity. If you put two things close together, you get crosstalk. If I lay in 100 traces adjacent to a certain plane, they couple (really well) to the plane. For example, suppose a 50-ohm trace passes adjacent to the 1.2V supply for a distance of 3 inches. For short edges, you get an instantaneous impedance of 50 ohms to the nearest reference plane wherever that trace goes. In this case, for any edge on the order of ½ ns (3 inches) you get a full 50-ohm coupling straight from the trace to the plane, and vice versa. On that scale of time, noise on the plane enters the trace effortlessly, and signals on the trace enter the plane according to the ratio of plane impedance (very low) to trace impedance (50 ohms). For example, suppose the 1.2V plane impedance to ground in that vicinity were 0.1 ohms. The coupling from trace to plane equals 2.5V*(.1/50) = 5 mV. Now try the same trick with 100 traces. You'll get 500mV of noise coupled into the 1.2V power system. That is not a formula for success.

I have also marked on this chart the position of the 2.5V mini-SMP test location we will use to measure the impedance of the power planes.

Trace Layout



DDR5
- TOP1
- GND2
- SIG3
- P4 3.3V
- SIG5
- P6 2.5V

DDR8
- P7 1.8V
- SIG8
- GND9
- SIG10
- GND11
- BOT12

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To help me get quantitative in the study of this board, Mark and Mike assembled some pretty fancy tools.

Mark took the hardware route, building physical boards and measuring them (along with Austin Tavares) using a LeCroy 6 GHz probe, sampling at 20 Gs/s, and an Agilent vector network analyzer VNA.

I like using the VNA, a frequency-domain tool, for power system analysis because it has incredible sensitivity, and can see the tiny effect on a plane caused by one 50-ohm source. If you could hook up 100 of these to the planes (like what happens in a real system) you could observe the same effects in the time domain with a scope, but since we are usually limited to a single 50-ohm source for testing, the VNA makes sense.

Mike whipped out his Ansoft simulation suite, consisting of three tools:

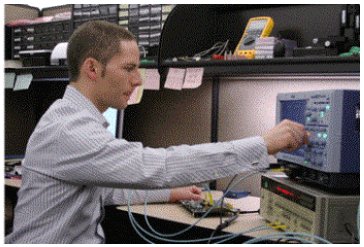
SIwave is a frequency-domain, s-parameter extractor. It looks at a complete layout (package, board stack, Gerbers, everything), and extracts s-parameter matrices for further analysis.

The Nexxim tool is a new transistor level circuit simulator that combines both time and frequency domain results. It takes in spice models for drivers and receivers and combines them with s-parameter blocks gleaned from 3D extraction tools, VNA measurements, w-element models and IBIS models to synthesize very complex circuits topologies.

The DesignerSI is a schematic tool used to compose circuits for analysis by Nexxim.

Our first step was to measure (and simulate) the impedance from 2.5V to ground at our top-and-bottom mini-SMP test point.

Tools used



Hardware

Agilent 8753ES VNA

LeCroy SDA6020 scope

Mark Alexander
Application Engineer
Xilinx Corp.

XILINX®

Software

ANSOFT

SIWAVE™
NEXXIM®
DESIGNERSI™

Michael Brenneman
Director, Packaging and PCB
Ansoft Corporation

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Here is our first result. It shows S21 (transmission gain) as measured top to bottom at the 2.5V mini-SMP location. The chart shows both measured and simulated data, using Ansoft SI-wave. The match between simulation and measurement looks quite reasonable for our work, so based on this agreement we may begin extrapolating with the SIwave simulator to show impedances at other locations on the card, locations we can't really probe, like "on the die". That's one of the cool advantages of simulation.

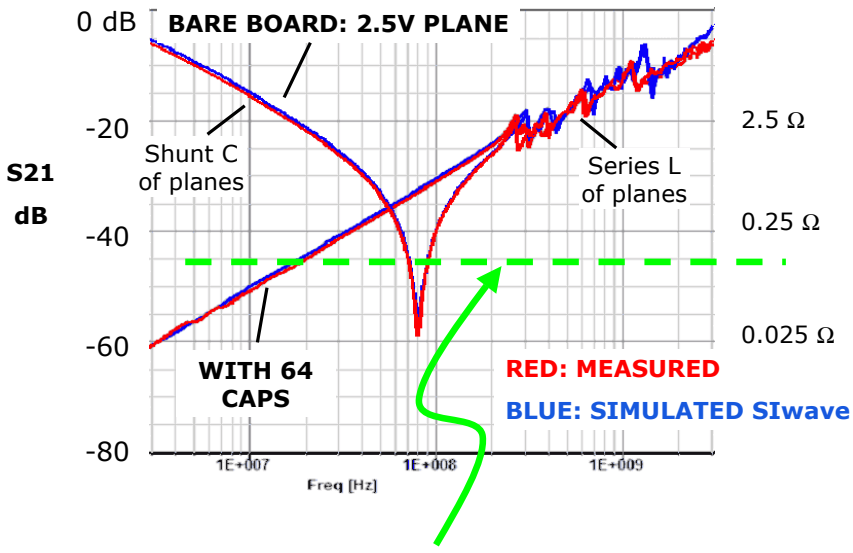
A "target impedance" is indicated on the chart. That's the level of impedance we need, system-wide, to handle 32 data lines at 20 mA each, if we want to limit the power-supply noise to 96 mV peak.

Notice that I said "system-wide". This measurement is taken at only one location: the mini-SMP. If you jam all your current through that one little hole, the chart shows what voltage noise you would have right *there*. A real FPGA, of course, does not jam all the power supply current through one tiny little hole, *it spread the current out* over many (hundreds) of power-and-ground pins on the bottom of a big BGA package. Spreading out the current you would perceive a lower overall impedance than measuring it my way, all at one point.

A single-point-of-contact measurement like I just did concentrates all the current in one place, creating very intense magnetic fields, and thus a lot of series inductance.

If you concentrate force a similar thing happens. Punch your fist into the surface of the water at a swimming pool. At one concentrated spot, the water feels soft. Now go to a 3-meter diving board and try a belly-flop. When you spread the load, water feels a *lot* harder (and it can rip off your swimming trunks!)

S21 Results at Mini-SMP Location



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In this measurement, I will admit that the magnitude of the "series inductance of the planes" surprised me.

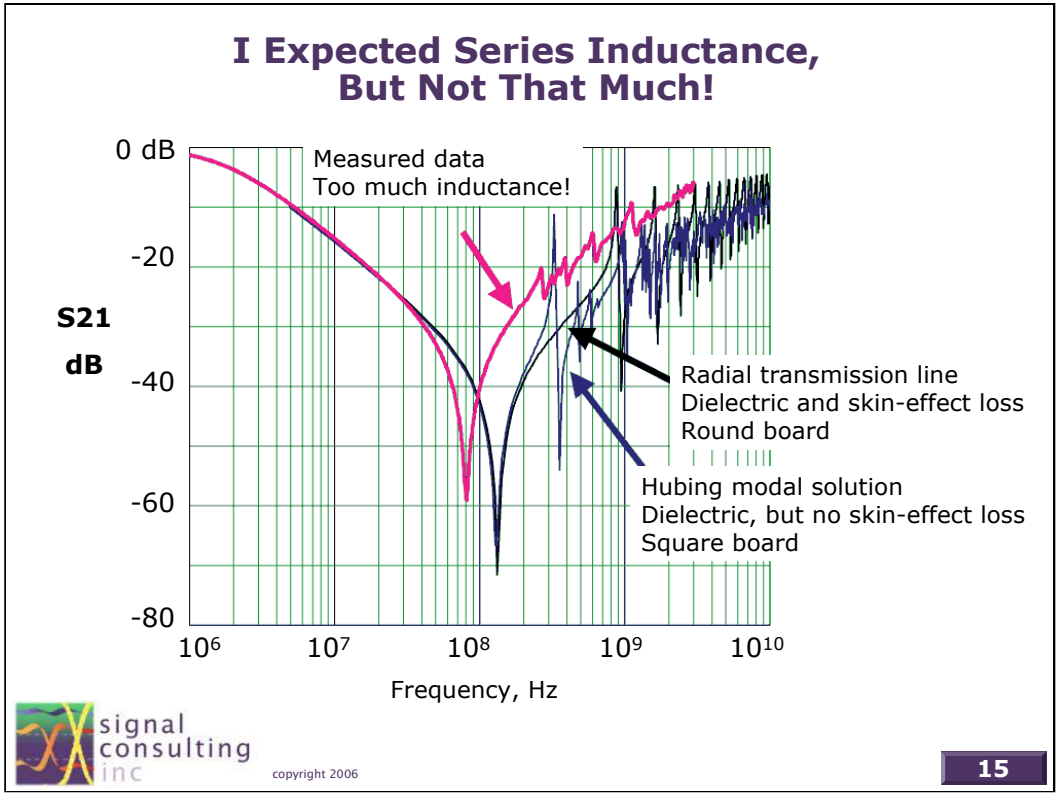
I expected a lower value, by about 5 dB. The plot shows the basis of my expectation. It depicts two approximations for spreading inductance.

(1) Radial transmission line method (a.k.a. the pizza slice method), and

(2) Multi-mode approximation published by Todd Hubing [1].

My two approximations match fairly well. The measured data (also simulated) appears above them, in purple. Above 1 MHz the measured data is about 5 dB higher.

The additional inductance represented by this difference turned out to be due to a layout problem at the mini-SMP location. I'd like to show you what happened.



[1] Minjia Xu, Yun Ji, Todd H. Hubing, Thomas P. Van Doren, James L. Drewniak, "Development of a Closed-Form Expression for the Input Impedance of Power-Ground Plane Structures", IEEE EMC Symposium 2001

[also see] Howard Johnson, "Short-Term Impedance of Planes" www.sigcon.com/Pubs/news/6_05.htm

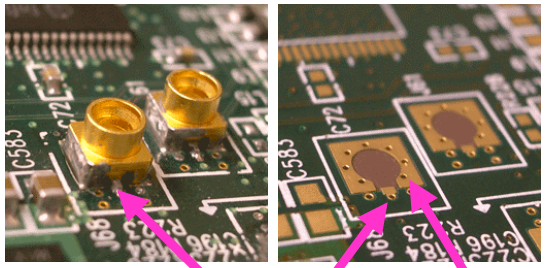
This is a *great example* of what can go wrong doing these measurements.

At top right you can see the Rosenberger connector we use, and also the land pattern underneath the connector. The signal pad sticks out to one side, so you can solder it by hand (a nice advantage for lab work).

The Rosenberger layout guidelines stipulate a plane-layer clear-out underneath the connector to relieve mounting-pad capacitance. This clear-out reaches all the way down through every plane layer.

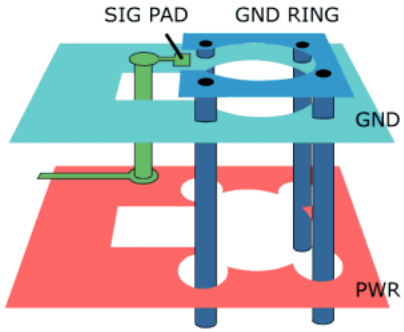
But… in our case we WANT to connect to power plane layer P6 (red).

Mini-SMP Guidelines



Signal pad

Ground ring



Rosenberger layout guidelines stipulate plane-layer clear-outs on every layer to relieve mounting-pad capacitance.

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In this picture I have omitted some of the ground layers, so you can clearly see what happened at the power layer in our application. On the solid layers you can see the clear-out region, with additional clearances to allow the ground vias to pass through layer P6 without touching.

Layer P6 is cut out around the mini-SMP signal via, per the Rosenberger guidelines.

The connection to layer P6 is diverted from the keyhole through a short connecting trace to a *second via* that establishes the actual connection.

What we are measuring in this case is a combination of:

(1) The plane P6, in series with

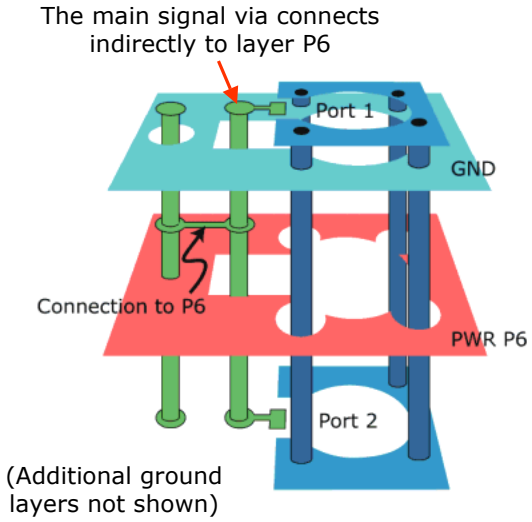
(2) The series inductance of the little connecting trace.

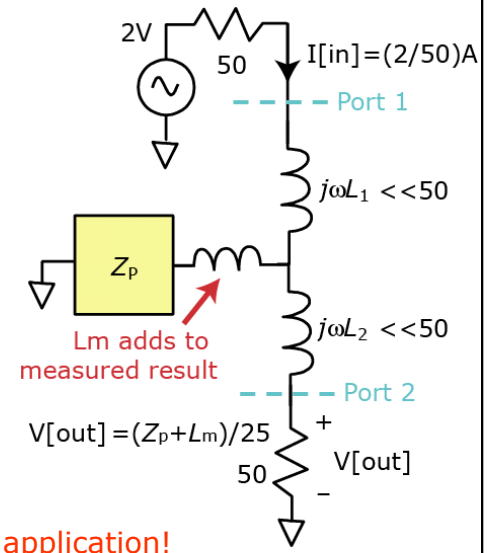
The schematic at right depicts the electrical situation. Inductor Lm represents the connecting trace. The is a beautiful 2-port measurement setup, but it's measuring Zp+Lm, not what we want to see.

In our measurements, the series inductance of the connecting trace increased our measured results by about 5 dB (almost double the impedance we were trying to measure).

This is one circuit that is OK to interpret mechanically. If I strike the top via pad (port 1) with a hammer, the force translates straight down to port 2, restrained not by plane P6, but merely by the mechanical stiffness (inductance) of the connection to P6.

OOPS! Layout Error





Not good in this application!

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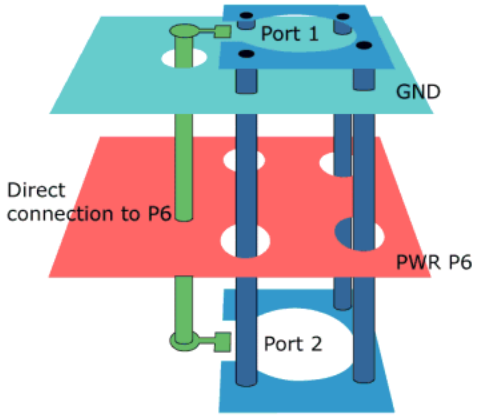
To fix the situation we have got to tie the signal via *directly* to layer P6.

For a power measurement application, no cutouts are necessary (or desirable).

The extra parasitic capacitance of the signal pad to the surrounding ground material does not affect measurements of power systems, because you are measuring such a HUGE low-impedance structure anyway.

Correct Layout for Power-Plane Impedance Measurement



(Additional ground layers not shown)

Each port proceeds directly to the power plane. No cutouts.

Do not pass GO, do not collect $200.

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Let's compare our measurement to a simplistic, lumped-element model for power system impedance. This model just takes the equivalent R, L and C for each capacitor in the power system and lumps them all together in parallel. It represents the effective impedance a fully distributed signal source, made of thousands of little sources spread out across your pcb, might experience.

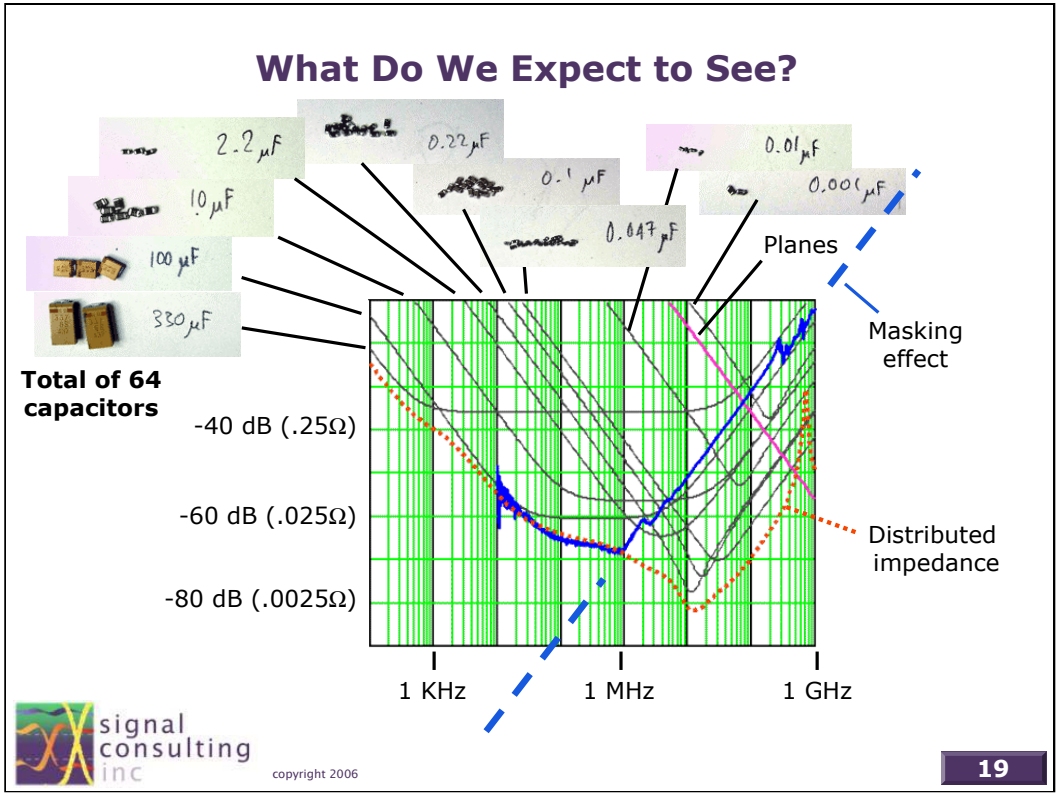
The 2.5-volt plane on the ML405 card is populated with a mishmash of 9 different capacitor types, totaling 64 discrete capacitors.

The picture shows the size (and number) of each type, along with an individual impedance graph for that type. For example, check out the curve for the 330uF type. It's the furthest left of the black curves. Since there are two of those components on the board, its aggregate curve shows a capacitance of 660 uF (and ESR of minus 37dB relative to 25 ohms, or about 0.35 ohms).

The overall lumped-element impedance curve is the parallel combination of all types (red dotted line). It tends to follow along the lowest of the individual curves at any given point. You can see in this graph that some of the capacitor types on this board probably aren't helping very much.

This type of graph is an excellent way to identify redundant (useless) capacitor types.

The measured curve (blue) matches the lumped-element approximation up to 1 MHz, but above there the curve measured at our mini-SMP location rises sharply because of the series spreading inductance of the planes. This spreading inductance masks the true distributed impedance of the planes.



You may have the greatest low-impedance capacitors in the world on your board, but you can't see them from one mini-SMP location—unless they are really close.

Spreading inductance is a function of distance (and also plane separation).

If you place capacitors *really close* to the mini-SMP location, close enough to significantly reduce the spreading inductance from the mini-SMP over to that spot, then the measured impedance would go down.

The rules for how close, and how much is the spreading inductance, are given in my article "Parasitic Inductance of Bypass Capacitors", (see reference at end of this presentation).

Impedance Masking

The spreading inductance of the planes (plus our layout error) acts in series with the true distributed impedance of the planes, masking it's true value.

Result: we can **not** observe **distributed** plane impedance from our single point of measurement.

What we **can** do: use a simulator to tell us what is the actual power impedance experienced *at the die, where it matters*.

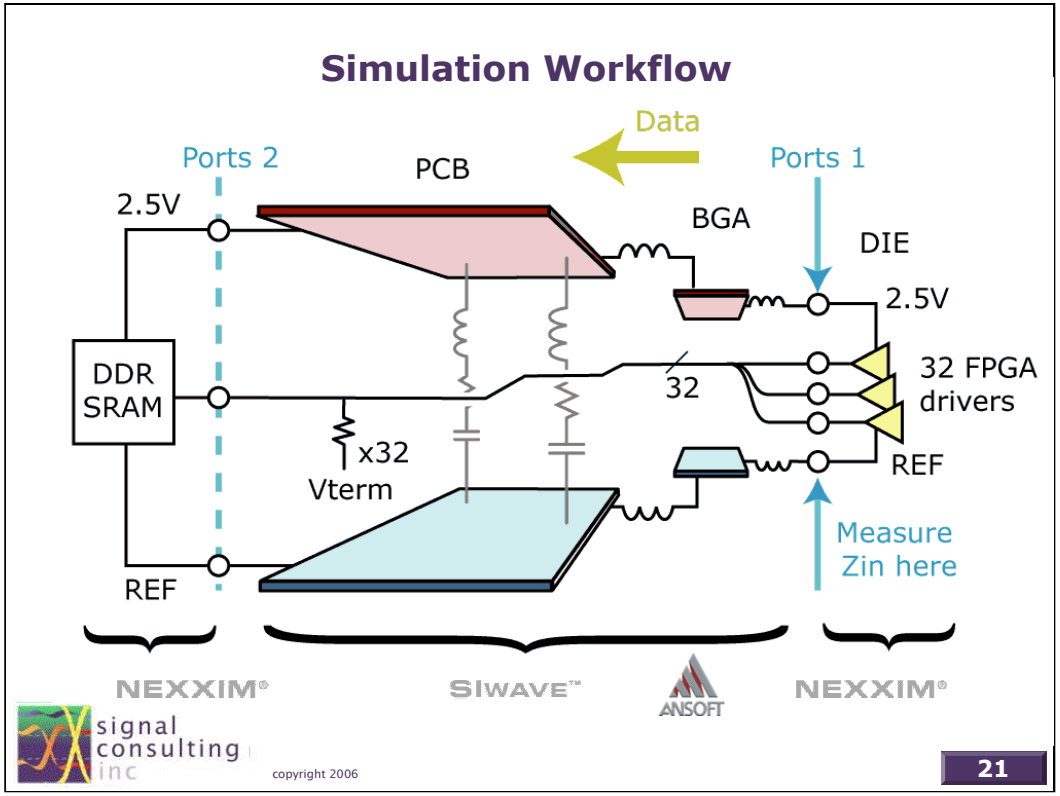
The particular setup I have chosen here focuses on the simulation of SDRAM write cycles. Mike configured 32 FPGA drivers at the die (right side of diagram), and they are set to blast bursts of data to the SDRAM on the left.

To begin simulating, Mike divides the system into parts.

First he uses SIwave to extract an S-parameter model representing the distributed passive circuitry. That includes the BGA substrate, its attachment to the pcb, the pcb itself, and all the bypass capacitors on the board.

Then he uses Nexxim (Spice engine) to combine that model with non-linear device models.

The resulting combination of tools should be able to show us the voltage/currents anywhere in the system.



Here is our first result. This time-domain waveform shows the voltage received at SDRAM location D6. The data write speed is 100 Mb/s.

On the left I show a measured waveform that Mark captured with his 6 GHz LeCroy probe, at 20 Gs/s.

On the right I show a portion of the simulated Nexxim waveform.

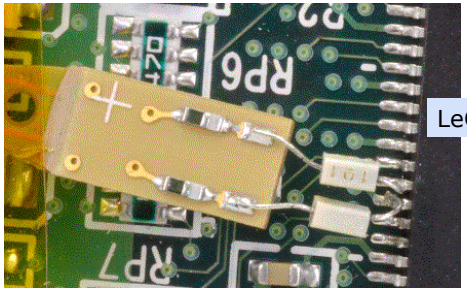
The measurements match reasonably well, although the simulated driver has a hotter (faster) edge than the real-world driver, causing more high-frequency wrinkles.

You can see that the signal amplitudes are comparable, indicating that the drive strength is set correctly. If you look right after each falling edge you can see a little blip of undershoot. That is the reflection from the SDRAM receiver capacitance.

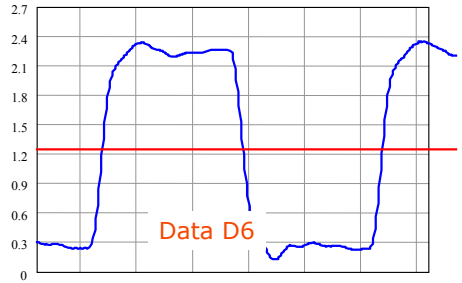
The timing of this blip, and the area underneath it are comparable on the two waveforms. That indicates that we have configured the correct line delay, impedance, and capacitive loading (SDRAM) at the end of the simulated transmission line.

We have some further work to do to isolate what causes the difference in rise/fall time.

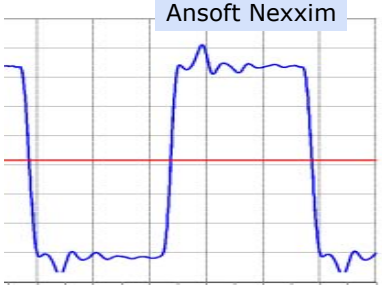
Calibration: Waveforms at DDR SDRAM



LeCroy 6GHz probe



Ansoft Nexxim



Faster edges from Spice model

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Now that we have our simulation environment built, let's play around! The following calculations are done just using SIwave (so the SPICE model irregularities won't matter).

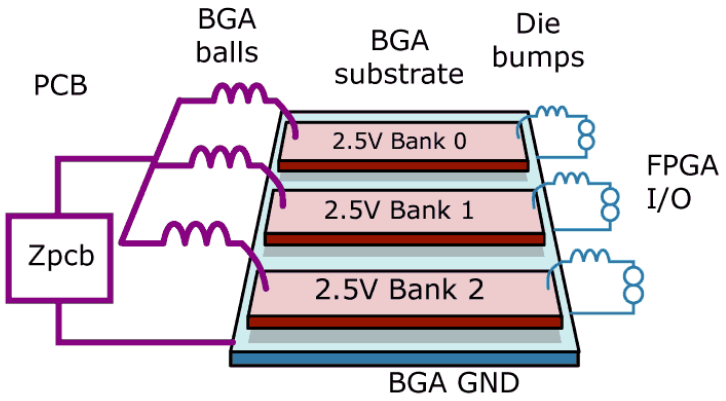
Here we are looking just at *power connections* within the BGA substrate, no signals. The I/O supply voltages for each I/O bank are conveyed separately inside the BGA package to the die power terminals for each bank. That way, you can power some I/O banks with 2.5V and others with 1.5V, according to how you wire up the power balls on the BGA package.

On the right side of the diagram, power terminals from the die connect (through bump inductances) to the various I/O bank voltage planes within the BGA substrate. I show three I/O band voltage planes in this picture. In a real part there are more.

When the drivers pop high, they draw current from the I/O bank power supply planes. We can model this action as a collection of tiny current sources, one for each I/O bank.

If all banks drive at once we can simplify the circuit further. If all banks drive at once they all react the same way, with the same voltage glitches. In that case, for the purpose of analysis, you can place all the I/O banks in parallel. For our next series of measurements, I'll do just that. In simulation, what you do is "group" all the 2.5 volt nodes on the die and drive them with one big source. Drive in a known current, measure the voltage developed across that source, and the ratio of voltage to current is defined as the aggregate input impedance of the power system at that point. That type of measurement is known to you s-parameter gurus as an S11 measurement.

Configuration of BGA 2.5V Planes



The I/O bank supply voltages are each conveyed separately inside the BGA package.

Here I use the S11 technique to show the aggregate impedance between 2.5V and ground, measured at the die bumps (with no die present). All IO bank VCCO supplies are driven together in this measurement, as if all active at once.

This is the way an ordinary BGA package operates, assuming it has flip-chip attachment and solid power/ground planes within the package.

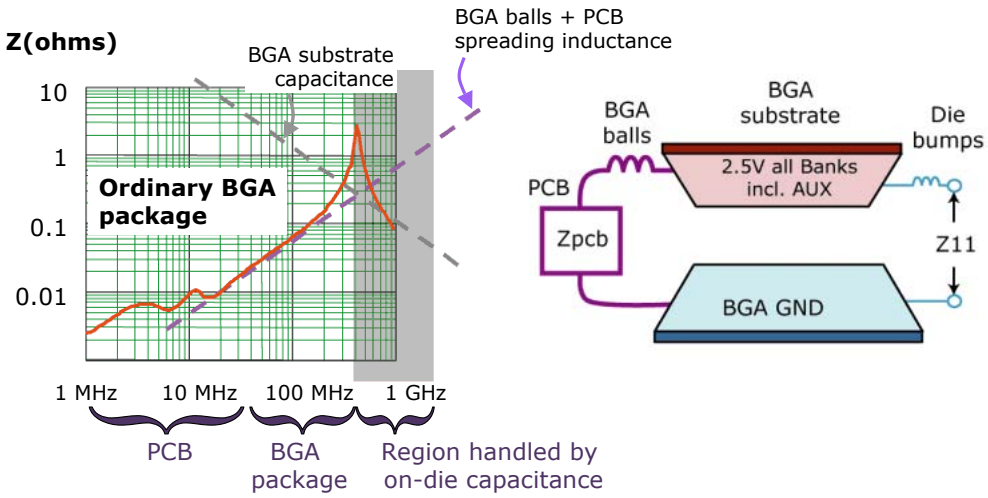
Notice that the system suffers from "spreading inductance" just like our mini-SMP location. That is the central insight of this presentation.

If you can't see all those wonderful low-inductance capacitors from a mini-SMP location, *then you can't see them from your die, either*.

To reduce the spreading inductance between your die and the bypass capacitors you can do two things: bring the pcb planes closer together, or bring the capacitors closer to the die. Of the two techniques, bringing the capacitors closer to the die is the more effective.

Let me show you.

From Die Looking Out to the PCB



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Here I have installed bypass capacitors inside the BGA package, right next to the die.

These capacitors within the BGA package significantly reduce the impedance presented to the die. With these additional capacitors present, the impedance observed at the die drops by 14 dB.

In this package, the BGA substrate and its capacitors handle all noise-control issues above 30 MHz.

This is the technique used in the Xilinx Virtex-4 FPGA. Bypass capacitors inside the BGA package, right there next to the die, protect the power system from excessive noise.

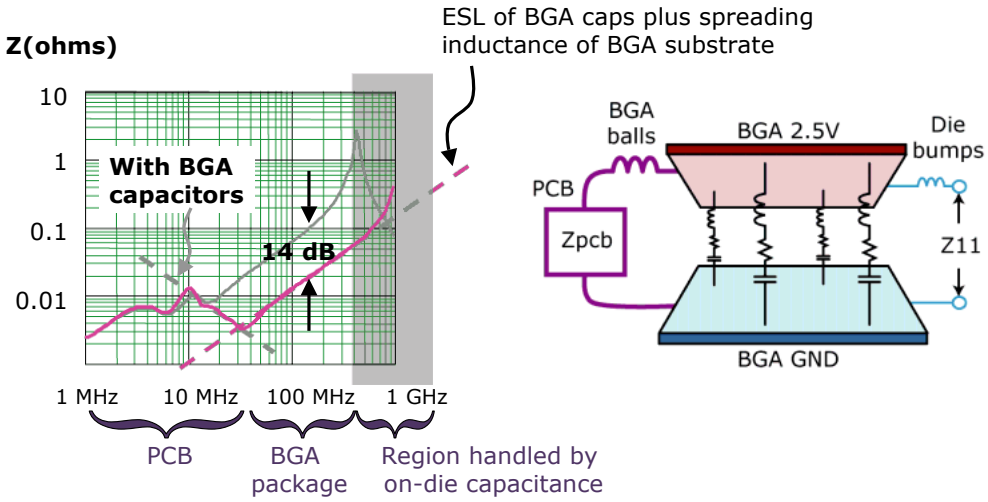
There is a third level of power-system protection built into the Virtex-4 FPGA, and that's the die capacitance. Every I/O circuit includes intentional on-die capacitance to help bolster the power system.

The transition from BGA-substrate power control to die-capacitance power control happens in this package somewhere around 400 MHz.

With these techniques, your FPGA power system is going to work even if you move to a Balkan state with an terrible power-system infrastructure.

The FPGA itself provides the low-impedance connections you need to provide adequate die powering at frequencies above 30 MHz. All the PCB has to do is cover the territory below 30 MHz.

Add BGA Capacitors



The BGA capacitors sit close to the die, hence the inductance reaching over to them is 14 dB less than if you have to reach all the way out onto the PCB to find your bypass caps.

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To demonstrate that, let's try an experiment. We are working with a simulator, so we can do anything we want, right? Let's try something wild. What if I remove the PCB?

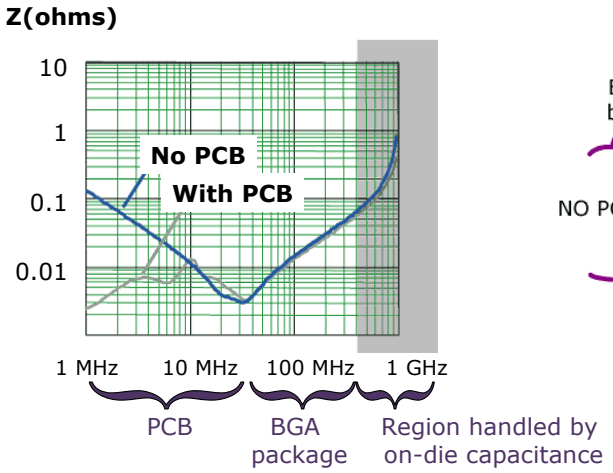
This diagram shows that even with the PCB completely removed, the capacitors within the BGA substrate provide a safe driving-point impedance for operation of the IO circuits at all frequencies down to 30 MHz.

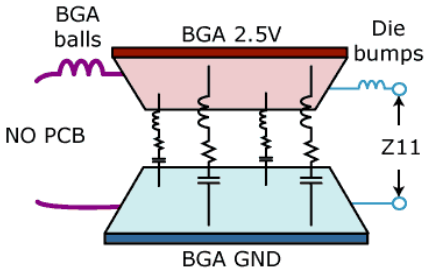
In this design, the PCB affects power supply noise at the die only at low frequencies. Above that, the BGA package, and then the die itself, take over.

As far as powering the die is concerned, the PCB need only provide a low-impedance connection between power and ground at frequencies BELOW 30 MHz. The FPGA package, in one easy-to-use, compact circuit, gives you all the protection you need above that frequency.

What about the other two power applications I mentioned at the beginning of this talk? High-frequency PCB bypassing may still be needed if you change reference layers on your board, or implement discrete end terminations. Those issues are not affected one way or the other by on-package capacitors.

What if the PCB Were Missing?





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Well, I'm about out of time today.

I hope I've provided some useful information to you about power system measurement methodology and its limitations, especially the issue of spreading inductance and how that limits your view of a distributed power system.

My central point is that you can't see all those good, low-inductance bypass capacitors on your board from any one point – and neither can your FPGA die – unless the capacitors are extremely close to the die.

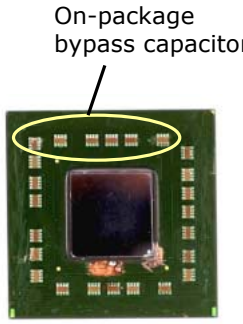
I showed the use Ansoft SI-wave and Nexxim tools to analyze power system performance. Thank you, Mike, for providing the simulation work for this presentation.

Finally, I conveyed to you my understanding of how on-package bypass capacitors work, and why they are useful.

Wrap-up

Demonstrated:

- Power system measurement methodology and limitations
- Ansoft SI-wave and Nexxim tools analyze power system performance
- How on-package bypass capacitors work, and why they are useful



Xilinx Virtex-4
BGA package with lid removed
showing in-package bypass capacitors

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For Further Study

Xilinx

- www.xilinx.com/signalintegrity
  Resources useful for high-speed designers
- www.xilinx.com/virtex4/si
  My SI tutorials for Xilinx RocketIO™ serial transceivers, also "BGA Crosstalk"—now available on DVD

Ansoft

- Combined time-frequency domain simulation
  www.ansoft.com/products/hf/nexxim/
- PCB S-parameter extractor
  www.ansoft.com/products/si/siwave/

Dr. Johnson: www.sigcon.com

- "Parasitic Inductance of Bypass Capacitors"
  www.sigcon.com/Pubs/edn/ParasiticInductance.htm
- "Parasitic Inductance of Bypass Capacitor II"
  www.sigcon.com/Pubs/news/6_09.htm
- Index to articles by keyword (look for "power")
  http://www.sigcon.com/pubsIndex.htm

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At this time I would be pleased to consider any questions or comments you may have.

Dr. Howard Johnson

Seminar schedule:

Oxford University
June 27-30, 2006,

returning to the U.S. for more courses in the fall.
www.sigcon.com

Your Questions?

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Extra slides for Q&A or other purposes

DDR SDRAM data signal at DDR D6 location

Agilent VNA screenshots at 2.5V mini-SMP location

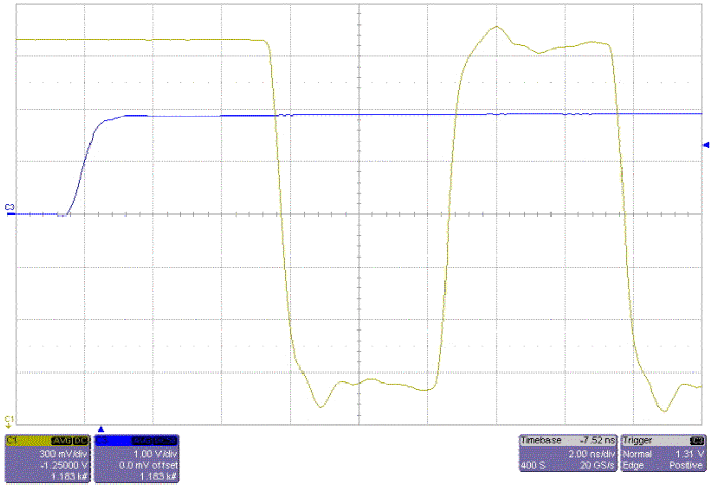
- Bare PCB
- All caps and no IC's

SIwave S21 screenshots at 2.5V mini-SMP location

- Bare PCB
- All caps and no IC's

Article: "Parasitic Inductance of Bypass Capacitors"

Data Signal at DDR SDRAM



LeCroy scope, 6 GHz probe, 20 Gs/s

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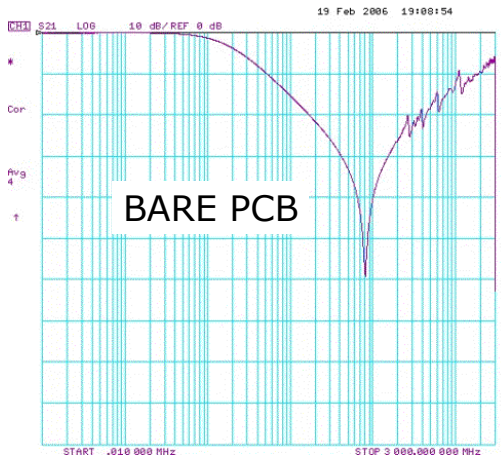
Agilent VNA at 2.5V mini-SMP



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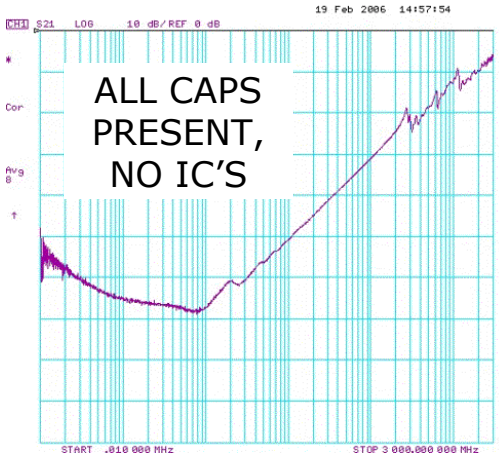
Agilent VNA at 2.5V mini-SMP



ALL CAPS PRESENT, NO IC'S

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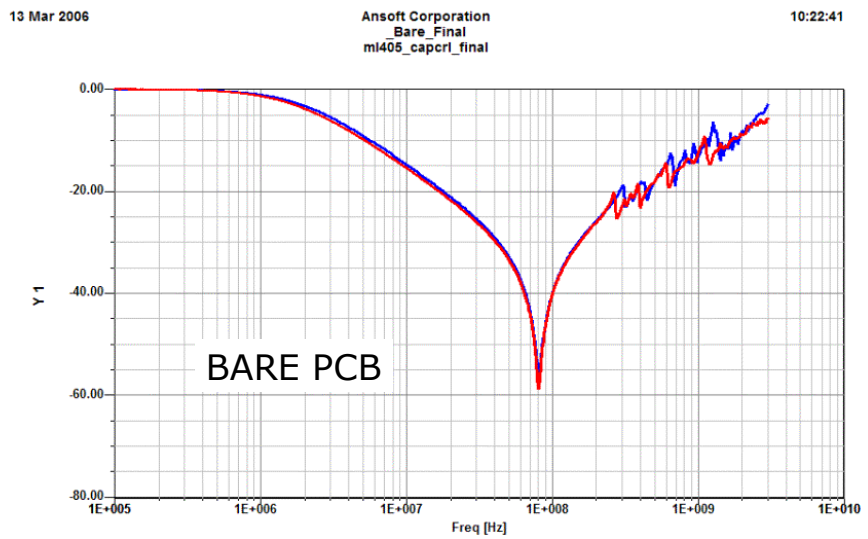
SIwave S21 at 2.5V mini-SMP



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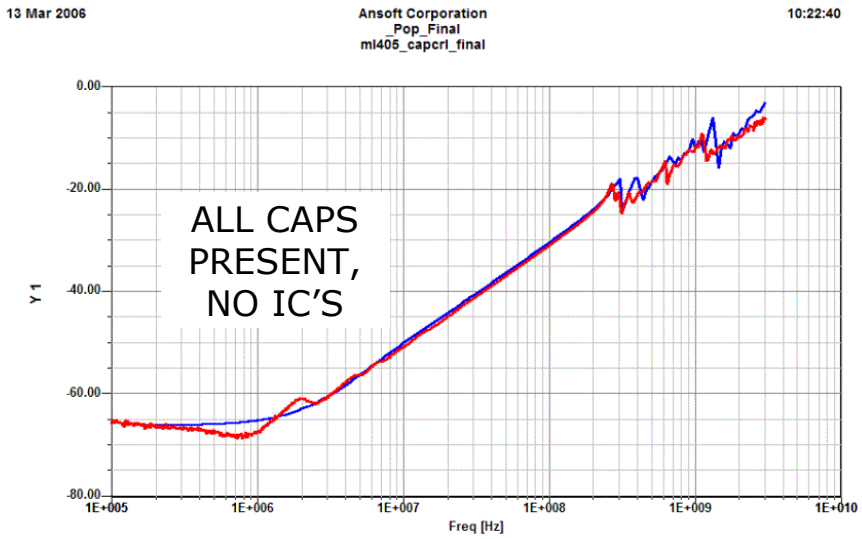
SIwave S21 at 2.5V mini-SMP



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Parasitic Inductance of Bypass Capacitor

First published in EDN Magazine July 20, 2000

Howard Johnson, PhD

You can estimate the parasitic series inductance of a bypass capacitor in a multilayer board with solid power and ground planes. You will need an approximation for the inductance L_1 due to the capacitor layout Figure 1, (green shaded region). Then, assuming that you have connected your bypass capacitor and your chip straight to the planes, another approximation for the spreading inductance L_2 represented by the volume of magnetic flux trapped between the planes (blue region). Finally, you might want to consider the inductance, L_3 , of the chip package itself (red region). The internal details of the construction of a monolithic ceramic capacitor itself add little to the total inductance.

The chip-package inductance (red region) is the least troublesome of the parts. Considering the chip's power and ground pins as a source of noise, the impedance of this source is much larger than the impedance between power and ground on your board. (If it were not, your board would have so much power-supply noise that it wouldn't work.) Therefore, the chip tends to act as a fixed source of current, independently of L_3 . In other words, L_3 affects the power-and-ground bounce that your chip experiences but not the noise coupled onto the power and ground planes.

The chip power-supply currents flowing through the impedances of L_2 and L_1 generate most of the high-frequency power and ground plane noise emanating from the structure in Figure 1. Power and ground plane noise in the frequency region that the bypass capacitors control varies in proportion to L_2+L_1 .

To compute the spreading inductance L_2 (blue region), assuming that the field intensity generated between the planes due to a single via with diameter D falls off inversely with distance and is independent of height, use

$L_2 = (\mu_0/\pi)(H_2)\ln(2S_2/D)$.

With H_2 expressed in inches, the quantity μ_0/π equals 10.16 nH.

The L_1 computation (green region) divides into two parts; the part of the inductance due to the capacitor body and its pads, and the part due to the vias. The combination of body, surface-mounting pads, and via pads (assuming that the vias are jammed right up against the mounting pads) comprises a long, wide structure that resembles a transmission line. For example, a 0603 mounting structure is approximately 30 mils wide, 120 mils long (via center to via center), sitting at some height, H_1, above the nearest solid reference plane.

Given the characteristic impedance, Z_0, for a structure with this width and height, and the time delay, T, corresponding to its length, you may approximate the inductive contribution due to the body and pads (ignoring fringing fields at the ends) as $L_1(\text{body}) = Z_0 T$. You can use any ordinary transmission-line calculator to approximate Z_0 and T. Next, approximate the inductive contribution of the vias at the ends using the Biot-Savart law integrated over the blue region, assuming the vias represent tiny current elements. The result is

$L_1(\text{vias}) = (\mu_0/2\pi)(H_1^2)(2/D - 1/S_1)$.

Add the body and via contributions to find the total, L_1. This approximation works only for S much larger than D .

Figure 1 graphically depicts calculations for a 0603 layout, with the vias jammed up against the capacitor mounting pads. The figure shows the total inductance, L_1, versus height.

A simulator does these calculations for you.

The assumed pad width is 30 mils, the total structure length (via center to via center) is 125 mils, and the via diameter is 12 mils. The x-marks show actual measured results. The value of L_2 for this structure, assuming S_2=0.500 and H_2=0.005 is 0.22 nH. Both L_1 and L_2 vary strongly with height.

If you mount the capacitor on the reverse side of the board, you have to sum the various inductances L_{2A}, L_{2B}, and others (yellow regions), thus illustrating a disadvantage of backside mounting.

If you must use traces to connect the capacitor vias connect to the capacitor mounting pads, add the inductance of those traces to L_1. At roughly 10 nH/in. for typical pc-board traces, the extra trace inductance quickly adds up. For example, 0.050-in. long traces at each end of a standard 0603 component adds around 1 nH to the completed layout inductance, substantially raising L_1.

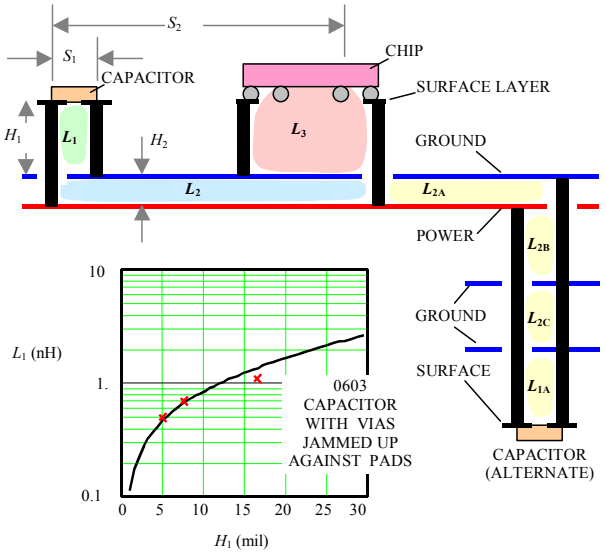

Figure 1—The inductance L_1 of a bypass capacitor layout varies strongly with height H_1.

Thanks for watching.